REMARKS

Applicant respectfully requests reconsideration of the present application in view of the reasons that follow.

No claims have been amended. Claims 1-6 remain pending.

Rejection under 35 U.S.C. § 102

Claims 1-6 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,657,291 to Podlesny et al. ("Podlesny"). Applicant respectfully traverses this rejection for at least the following reasons.

Independent claim 1 is directed to a register file and recites "each of said first AND gates in one of said input port selector receives a write instruction signal for specifying whether or not write data input through a corresponding one of said input ports is to be stored in a corresponding one of said registers, and generates a logical product of said write data and said write instruction signal and an inverted signal of each of said write instruction signals received through said input ports each having a higher priority order compared to said input port corresponding to said one of said input port selector." Podlesny fails to disclose at least this feature of claim 1.

Podlesny discloses a multiport register file memory cell including decoder ports 16-1 through 16-N which present addresses to select and priority circuit 12, where the read addresses RA1 through RAN are presented to respective of the decoder ports. If the same address is presented to more than one decoder port, the select and priority circuit 12 determines which of the decoder ports has the higher priority to access a desired memory location of memory cell array 18 (col. 4, lines 8-16).

In contrast to the input port selector as recited in claim 1, however, the select and priority circuit 12 of Podlesny does not include AND gates which are configured to generate "a logical product of said write data and said write instruction signal and an inverted signal of each of said write instruction signals received through said input ports each having a higher

priority order compared to said input port corresponding to said one of said input port selector." While the select and priority circuit 12 of Podlesny includes AND gates 42-1 through 42-N/2, the inputs to these end gates are the outputs from the decoder circuits, i.e., decoded addresses, not write data or any inverted signal of a write instruction signal. Moreover, Podlesny fails to disclose any inverted signal input to the AND gates 42-1 through 42-N/2, much less an inverted signal of a write instruction signal. In sum, the structure of the Podlesny select and priority circuit 12 is very different from that of the input port selector as recited in claim 1.

Podlesny also fails to disclose or suggest all the features of independent claim 5. Independent claim 5 comprises "a plurality of read data selectors each corresponding to one of said output ports, each of said read data selectors including AND gates in number corresponding to said a number of registers and an OR gate generating a logical sum of outputs from said AND gates, each of said AND gates generating a logical product of data stored in a corresponding one of said registers and an activating signal which assumes a high level when said corresponding one said registers is specified." Podlesny fails to disclose the read data selectors of claim 5.

Podlesny discloses read address comparators 14 and a data transfer unit 20 which operate to ensure that data from the memory cells of the cell array 18 is placed on the bit lines corresponding to the non-selected lower priority decoder ports 16-1 through 16-N (col. 4, lines 22-29). The address comparators 14 and data transfer unit 20 of Podlesny do not have the structure as the plurality of read data selectors as recited in claim 5. Figures 4A and 4B of Podlesny illustrate the address comparators 14 and data transfer unit 20. As can be seen, however, this structure does not include "AND gates in number corresponding to said a number of registers and an OR gate generating a logical sum of outputs from said AND gates" as recited in claim 5, much less "each of said AND gates generating a logical product of data stored in a corresponding one of said registers and an activating signal which assumes a high level when said corresponding one said registers is specified" as further recited in claim 5. If the Examiner maintains the rejection based on Podlesny, applicant respectfully

requests that the Examiner specifically point out the AND gates of read data selectors in Podlesny.

The dependent claims are patentable for at least the same reasons as their respective independent claims, as well as for further patentable features recited therein.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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